

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Bruce B. Doris et al. Confirmation No.: 6189

Serial No.: 10/695,748 Group Art Unit: 2814

Filed: October 30, 2003 Examiner: T. Le

For: STRUCTURE AND METHOD TO ENHANCE BOTH nFET and pFET  
PERFORMANCE USING DIFFERENT KINDS OF STRESSED LAYERS

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

AMENDED APPELLANT'S BRIEF UNDER 37 C.F.R. §41.37  
AND RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

This amended brief responds to a Notice of Non-Compliant Appeal Brief mailed May 22, 2007, in regard to the brief filed February 16, 2007, and is in furtherance of the Notice of Appeal, filed in this case on November 17, 2006. The Notice of Non-Compliant Appeal Brief indicates that the brief filed on February 16, 2007 does not contain a mapping of claim 10 on the specification and drawings. This amended brief provides such a mapping, some minor editorial revisions, optional sub-headings for arguments presented in regard to dependent claims and a concluding summary paragraph but is otherwise identical to the brief filed February 16, 2007.

This amended brief contains these items under the following headings, and in the order set forth below (37 C.F.R. §41.37(c)):

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I. REAL PARTY IN INTEREST

The real party in interest in the appeal is:

- the party named in the caption of this brief.
- the following party:

International Business Machines Corporation of Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals, interferences or judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal:

- there are no related appeals, interferences or judicial proceedings related to, which directly affect or may be directly affected by or have a bearing on the Board's decision in this pending Appeal.
- these are as follows:

**III. STATUS OF CLAIMS**

The status of the claims in this application are:

**A. Total number of claims in Application**

Claims in the application are: claims 10 - 19

**B. Status of all the claims:**

1. Claims cancelled: claims 1 - 9.
2. Claims withdrawn from consideration but not cancelled: none.
3. Claims pending: 10 - 19.
4. Claims allowed: 13 - 15 (subject to being rewritten in independent form).
5. Claims rejected: 10 - 12 and 16 - 19.

(Note - claims 13 - 15 have been indicated to be directed to allowable subject matter and have been indicated as allowable "if rewritten to overcome rejection(s) under 35 U.S.C. §112, second paragraph, set forth in this action" and in independent form. The final office action of August 17, 2006, does not contain any rejection of claims 13 - 15 under 35 U.S.C. §112 or any other statutory grounds but, rather, an Examiner's statement of reasons for allowance of claim 13, from which claims 14 and 15 depend, is included in that final action.)

**C. Claims on Appeal.**

The claims on appeal are: 10 - 19.

(Note - The Advisory Action of November 6, 2006, indicates claims 10 - 19 to be rejected although no rejection is applied to claims 13 - 15 in either the Advisory Action or the final office action of August 17, 2006.)

IV. STATUS OF AMENDMENTS

The status of amendments filed subsequent to the final rejection are as follows:

The Advisory Action mailed November 6, 2006, indicates that the amendment filed October 17, 2006, will be entered for purposes of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention as defined in the claims on appeal, including the sole independent claim 10 and claims 11 - 19 depending therefrom, is directed to a structure, exemplary forms of which are illustrated in Figures 6 and 8C, for enhancing carrier mobility in field effect transistors (FETs), particularly in complementary pairs, by applying stress to the conduction channels thereof. However, different compressive or tensile stresses must be applied to nFET and pFET channels in order to achieve enhanced carrier mobility in these respective conductivity types of FETs since tensile stress enhances electron (the majority carrier in nFETs) mobility and reduces hole mobility while compressive stress enhances hole (the majority carrier in pFETs) and reduces electron mobility, as discussed on page 3, line 17+, of the specification.

A problem arises from the number of steps (including mask formation and removal steps) required to apply different materials by selective blanket deposition and selective material removal to produce such tensile or compressive stresses to transistors of different types, particularly when in close proximity and/or in complementary pairs. The invention as recited in the sole independent claim 10 provides a solution to this problem by inclusion of a shear force isolation dielectric layer 120 (see page 12, line 8, and Figures 5 and 6) or 12 (see page 14 and Figure 8C) which prevents or substantially reduces stresses from later applied layers from reaching the substrate where the conduction channels of the respective transistors are formed. By including such a shear force isolation layer, a later-applied, stressed layer may be left in place without affecting or otherwise reducing the substrate stress applied from a stressed layer (e.g. tensile layer 11) below the shear force isolation layer 120. Providing such a shear force isolation layer separating stressed layers (recited in the last two lines of claim 10) thus allows a stressed layer to overlie another stressed layer without compromising carrier mobility enhancement and for

selective material deposition or removal steps including masking steps requiring high overlay accuracy to be omitted.

Specifically, independent claim 10 recites (with parenthetical reference to exemplary portions of the specification and drawings):

10. A structure that adjusts carrier mobility (e.g. page 3, line 17+) in CMOS transistors (Figures 1 - 6 and page 9, lines 5 - 7) comprising:
  - a substrate (14, Figures 1 - 6, page 9, lines 20+),
  - a first transistor having a gate dielectric (205), gate electrode (208), and source, drain, and gate regions (19), formed on said substrate (nMOSFET 20, Figures 1 - 6, page 9, line 31 - page 10, line 9),
    - a second transistor having a gate dielectric (215), gate electrode (218), and source, drain, and gate regions (19), formed on said substrate (pMOSFET 21, Figures 1 - 6, page 9, line 31 - page 10, line 9),
    - a first film (11 - Figures 2 - 6, page 10, line 21+) providing tensile stress (page 10, line 26) at least at the channel of said first transistor,
    - a second film (13 - Figure 6, page 12, line 20+) providing compressive stress (page 12, line 30) at least at the channel of said second transistor, a portion of said second film extending in the same region of said substrate as a portion of said first film (Figure 6, page 12, lines 24 - 24), and
    - a shear force isolation layer (120 - Figure 5) separating said first film and said second film and said tensile and compressive stress therein (page 12, lines 27 - 34) in at least one area (e.g. nMOS 20).

Claim 11 additionally recites particular materials (e.g. page 10, lines 30 - 31) of the stressed layers, claim 12 recites that the shear isolation layer separates the stressed layers at all points of overlap (Figure 6, page 12, lines 7 - 9), claim 13 (apparently drawn to allowable subject matter) recites that the first stressed film is closer to the substrate than the second stressed film and does not fully surround the first transistor (Figure 6, page 14, lines 11+), claims 14 (depending from claim 13) and 18 recite that the shear force isolation layer is the only separation between the stressed layers (Figures 6 and 8c, page 12), claims 15 (depending from claim 13) and 19 further define the location of the isolation layer with reference to the second transistor gate (Figure 8b, page 14, line 23+), claim 16 recites that the isolation layer separates the stressed layers in selected locations (Figure 8b and 8c, page 14, line 3+) and claim 17 is similar to claim 13 but recites that the second film surrounds the first transistor (Figure 6, page 14).

**VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 10 - 12 and 16 - 19 have been rejected under 35 U.S.C. §102 as being anticipated by Hachimine et al. No other grounds of rejection are included in the final office action of August 17, 2006.

ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

No claims have been finally rejected under 35 U.S.C. §112, first paragraph

**ARGUMENT VII B. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH**

No claims have been finally rejected under 35 U.S.C. §112, second paragraph.

ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102

VIIC(1) Independent claim 10 and dependent claim 12

It is respectfully submitted that no claims in the application are anticipated by Hachimine et al. The Examiner asserts that layer 15 (Figure 24, illustrating an intermediate but not final product, or Figure 31) is a shear force isolation layer and, indeed, layer 15 is illustrated as separating oppositely stressed layers 14a and 14b in those Figures. However, in the embodiment (embodiment 1) including the process step illustrated in Figure 24 layers 14a and 15 are removed leaving only layer 14b over the p-channel MISFET avoiding any need for layer 15 to perform any function other than as an etch stopper as noted in paragraph [0207] of Hachimine et al. Note also the reference to removal of film 14a and the use of film 15 as an etch stopper in paragraph [0240}, specific to Figure 24. Moreover, paragraph [0214] of Hachimine et al. clearly states that the effect of one stressed film overlapping an oppositely stressed film will reduce the effect of the latter *unless the overlapping film is removed*; thus *clearly indicating that layer 15 is not expected to function as a shear force isolation film* or even recognizing that such a film or even such a structure could be produced. In regard to the embodiment of Figure 31 (embodiment 6) films 14b and 15 are left in place but the different tensile and compressive stresses are achieved by the stress from film 14b exceeding the stress derived from film 14a which can only be achieved if film 15 is *not* a shear force isolation film since the stress from film 14b *must necessarily be transmitted through both films 15 and 14a to the substrate, as explicitly noted in paragraph [0279].*

Other passages of Hachimine et al. which are inconsistent with layer 15 being a shear force isolation layer were pointed out in response to the final action of August 17, 2006, as follows (pages 7 - 8):

“In the present office action, the Examiner indicates that the previously submitted remarks summarized above are not found to be

persuasive since the Examiner finds it “apparent that the Applicant reads a “non-stressed” limitation of the oxide layer 12 or 120 into the claim” while no such limitation is recited therein and thus concludes that layer of Hachimine et al. “would be a shear force isolation layer” since it is located between oppositely stressed layers, as alluded to above. It is respectfully submitted that such a conclusion does not logically follow from the mere location of layer 15 particularly since paragraph [0214] of Hachimine et al. clearly, explicitly and unambiguously indicates that stresses are communicated from layer 14a to layer 14b (as identified in, for example, Figure 24) through layer 15 and compromises stresses in the channel which would otherwise result from layer 14b, thus *necessitating* the removal of layer 14a by *use of layer 15 as an etch stop* (as noted in paragraph [0207] - see also paragraphs [0220] - [0224]) to attain the desired result in the completed (as distinct from an intermediate stage of manufacture) device. It is clearly improper to conclude that structure in a reference is *other* than what it is disclosed to be or that it has properties *different from and opposite* those disclosed in the reference, particularly in a rejection for anticipation under 35 U.S.C. §102; for which it is required that the reference disclose the identical invention in *as complete detail as is contained in the claims* (see Richardson v. Suzuki Motor Co., 9 USPQ2d 1051, 1053, Fed. Circ., 1987, previously cited and to which the Examiner has not replied), even if “inherency” is not explicitly invoked by the Examiner.

“Further, contrary to the Examiner’s assertion that Applicant reads a “non-stressed” limitation into the claims which is not recited therein, there is no requirement that any portion of the recited shear

force isolation layer be non-stressed (although a non-stressed layer, as deposited, is disclosed to be “preferred” at page 11, lines 21 - 22) but only that shear forces on one side of it (e.g. due to compressive or tensile stresses) will not be transferred to a film on the other side of the shear force isolation film (as Hachimine et al. explicitly discloses will, in fact, occur across film 15 therein). Typically, this avoidance of transfer of significant forces across a film is achieved in accordance with the invention by providing a film of a suitable (e.g. low) density and exhibiting elasticity (or lack of rigidity) such that strain caused in the film by stresses (in shear) on one side of the film are not transmitted to the other side of the film to apply (in shear) stress in an adjacent structure but are accommodated by the elasticity or lack of rigidity of the “shear force isolation film”. This can be visualized by, for example, squeezing one end or side of a block of elastic material, such as an eraser, and observing that little, if any, distortion of the geometry occurs at an opposite end or side thereof. (In contrast, it should be noted that, in general, a film suitable for use as an etch stop, as film 15 is intended to function in Hachimine et al., should be of relatively high density and, hence, rigidity, to function acceptably as an etch stop; thus resulting in the problem which Hachimine et al. explicitly reports.)”

It is respectfully submitted that *none* of these passages of Hachimine et al. is consistent with layer 15 being a shear force isolation layer while *no passage consistent with a force isolation function is seen and none has been pointed out by the Examiner.*

The Examiner, in office actions prior to the final action of August 17, 2006, had improperly asserted inherency of the property of shear force isolation to layer 15,

*diametrically contrary* to the description of the function of layer 15 in Hachimine et al. and which was further shown to be improper by production of evidence showing forms of silicon oxide which do not inherently provide a shear force isolation function. While inherency has not been explicitly asserted in the final action of August 17, 2006, the Examiner still asserts that layer 15 is a shear force isolation layer simply by virtue of being interposed between oppositely stressed layers. It is respectfully submitted that such a position in support of a rejection for anticipation is not only clearly insufficient to do so but is clearly improper and utterly untenable. Again, the only embodiment of Hachimine et al. in which layer 15 appears to remain in the final product is embodiment 6 in which layer 15 clearly *must not be a shear force isolation layer in order to transmit stress from layer 14b to the substrate while overcoming the opposite stress derived from layer 14a.*

Therefore, it is respectfully submitted that layer 15 of Hachimine et al. is clearly not a shear force isolation layer answering that specific recitation in claim 10 and claims 10 - 19 are not, in fact, anticipated thereby.

#### VIIC(2) Dependent claim 11

Further, in regard to dependent claims, Hachimine et al. does not teach a *shear force isolation film* being formed of the claimed materials (although Hachimine et al. discloses silicon oxide for layer 15) as recited in claim 11. Therefore Hachimine et al. does not anticipate claim 11.

#### VIIC(3) Dependent claims 13 - 15

Moreover, Hachimine et al. does not teach or suggest the subject matter of claims 13 - 15 as admitted by the Examiner.

#### VIIC(4) Dependent claim 16

Hachimine et al. does not teach or suggest provision of a shear force isolation film between selected areas of the stressed films. On the contrary, as pointed out above, the film relied upon by the Examiner is a blanket film (in the intermediate

structure) which is removed in all areas in which the second stressed film is formed. Therefore, Hachimine et al does not anticipate claim 16.

VIIc(5) Dependent claims 17 - 19

Hachimine et al. does not teach or suggest a first stressed film *surrounding* a transistor or oxide liner (claims 17 and 19, respectively) or the top of a transistor gate being engaged by the second stressed film (claim 19). Claim 18 depends from claim 17. Therefore Hachimine et al does not anticipate claim 17, 18 or 19,

**ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103**

No claims have been finally rejected under 35 U.S.C. §103.

**ARGUMENT VII E. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112**

No claims have been finally rejected based on any statutory authority other than 35 U.S.C. §§102, 103 or 112.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. - 9. (Cancelled)

10. A structure that adjusts carrier mobility in CMOS transistors comprising:
  - a substrate,
  - a first transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate,
  - a second transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate,
  - a first film providing tensile stress at least at the channel of said first transistor,
  - a second film providing compressive stress at least at the channel of said second transistor, a portion of said second film extending in the same region of said substrate as a portion of said first film, and
  - a shear force isolation layer separating said first film and said second film and said tensile and compressive stress therein in at least one area.
11. A structure as recited in claim 10, wherein said first film and said second film can be composed of nitride, oxide, or other material that exhibits either tensile or compressive properties, respectively, corresponding to said tensile stress in said channel of said first transistor or said compressive stress in said channel of said second transistor.
12. A structure as recited in claim 10, wherein said first film and said second film are separated by said shear force isolation layer at all points of overlap.

13. A structure as recited in claim 10, wherein said first film; is closer to the substrate than said second film, and does not fully surround said first transistor, but rather the sides only, while the remaining surfaces of said first transistor are contacted by said shear force isolation layer.
14. A structure as recited in claim 13, wherein said shear force isolation layer is the only separation between said first transistor and said second film.
15. A structure as recited in claim 13, wherein said shear force isolation layer surrounds the majority of an oxide liner of said second transistor gate electrode except the top of the gate which engages directly with said second film.
16. A structure as recited in claim 10, wherein said first film and said second film are separated by said shear force isolation layer at selected areas.
17. A structure as recited in claim 16, wherein said first film, closer to said substrate than said second film, fully surrounds said first transistor.
18. A structure as recited in claim 17, wherein said first film is the only separation between said first transistor and said second film.
19. A structure as recited in claim 17 wherein said second film surrounds said oxide liner at the sides of said second transistor gate electrode with the top of the gate directly engaged with said second film.

IX. EVIDENCE APPENDIX

No additional evidence is relied upon in this Appeal.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings having a bearing of this Appeal.

### Summary and Conclusion

In view of the foregoing, it is clear that the Examiner has attributed a shear force isolation function to film 15 of Hachimine et al. solely based on the disclosure of silicon oxide for the film through hindsight and based solely on the present disclosure while numerous forms of silicon oxide are known (and evidence thereof provided in the record attached to the response filed December 13, 2005) films which do not exhibit such a property but can be used to impart or transfer stress as, in fact, is explicitly disclosed in Hachimine et al. By the same token and for the same reasons, attribution of such a property to film 15 of Hachimine et al. cannot be reached through a rationale of inherency, particularly in view of the disclosure at paragraphs [0214] and [0279] which clearly and explicitly indicate that stress is transferred through film 15 and that, in the latter case, Hachimine et al. clearly relies on that property *contrary to the stress isolation property claimed*. Accordingly, the Examiner has not made a *prima facie* demonstration of anticipation in regard to any claim on appeal and reversal of the Examiner's position in regard to the asserted sole ground of rejection is respectfully submitted to be in order and is respectfully requested.

Respectfully submitted,



Marshall M. Curtis  
Reg. No. 33,138

Whitham, Curtis & Christofferson, P.C.  
11491 Sunset Hills Road, Suite 340  
Reston, VA 20190  
Tel. (703) 787-9400  
Fax (703) 787-9400  
Customer No. 30743